by locking the output signal to a harmonic of the reference signal. (See Taylor, column 1, lines 55-68). There is no teaching or suggestion in Taylor for detecting "deviations of the PLL input signal's frequency outside a predetermined input frequency range" and "forcing the frequency of the PLL output to a predetermined frequency". Furthermore, it is impossible for the invention in Taylor to perform the claimed "forcing the frequency of the PLL output" to anything but a selected harmonic of the reference input signal.

Since Taylor fails to teach or suggest the claimed invention of claim 26, it is respectfully submitted that claim 26 is patentable over Taylor. Therefore, the Applicants submit that claim 26 fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claims 36 and 49 recite similar features as recited in claim 26. As such, the Applicants submit that independent claims 36 and 49 are not anticipated by the teachings of Taylor and also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

Furthermore, dependent claims 27-29, 37-39, and 50-51 depend either directly or indirectly from claims 26, 36, and 49 and recite additional features therefor. As such and for the exact same reasons set forth above, the applicants submit that none of these claims is anticipated by the teachings of Taylor. Therefore the Applicants submit that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

Conclusion

Thus the Applicants' submit that none of the claims, presently in the application, is anticipated under the provisions of 35 U.S.C. § 102 and that all of these claims now fully satisfy the requirements of 35 U.S.C. § 112. Consequently, the applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending n the application, it is requested that the Examiner telephone Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

E/Wall

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Dated: 1/23/02

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MARKED-UP CLAIMS

26. (Amended) A phase-locked loop (PLL) comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the [a] control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency [value], the control circuitry including beat frequency circuitry that detects deviations of the input frequency outside the predetermined input frequency range.

30. (Amended) A phase-locked loop (PLL) comprising:

an oscillator responsive to a control signal by producing a PLL output signal,

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the [a] control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency [value], the control circuitry including measurement circuitry which determines whether the PLL input signal's frequency deviates outside the predetermined input frequency range by measuring the voltage of said control signal coupled to the oscillator.

36. (Amended) An apparatus for providing a synchronized clock signal comprising:

a clock source that produces a clock output signal,

a PLL responsive to the clock output signal, said PLL comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the [a] control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency [value], the control circuitry including beat frequency circuitry that detects deviations of the input frequency outside the predetermined input frequency range.

40. (Amended) An apparatus for providing a synchronized clock signal comprising:

a clock source that produces a clock output signal;

a PLL responsive to the clock output signal, said PLL comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the [a] control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency [value], the

control circuitry including measurement circuitry which determines whether the PLL input signal's frequency deviates outside the predetermined input frequency range by measuring the voltage of said control signal coupled to the oscillator.

48. (Amended) A telecommunications network comprising:

a plurality of network elements at least two of which include a clock module that produces a clock output signal, and communications links connecting the network elements, the clock module of a first network element including a PLL connected to receive and to lock onto the clock output of another clock module within the network, the PLL comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the [a] control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency [value], the control circuitry including measurement circuitry which determines whether the PLL input signal's frequency deviates outside the predetermined input frequency range by measuring the voltage of said control signal coupled to the oscillator.